COS 397 Spring 2010 Class Exercise 2 *9 questions; 4 pgs.* *Due 2010-01-21 3:15 p.m.*

This exercise is designed to complement the paper on sorting in manycore GPUs[1] assigned as reading, with the goal of highlighting both the technical aspects and the presentation and research-conduct aspects as they relate to Capstone projects.

1. List the members of your group below:

2. What are coalesced writes and why are they important?

3. Explain the reasoning behind treating each thread block as a processor for the purpose of algorithm analysis.

[1] Nadathur Satish, Mark Harris and Michael Garland, "Designing Efficient Sorting Algorithms for Manycore GPUs," in *Proceedings of the 23rd IEEE International Parallel and Distributed Processing Symposium (IPDPS)* (Rome, Italy, 2009).

4. What is CRCW PRAM?

5. The paper does not list any code or pseudocode. How may we study the details of the implementations described in the paper, perhaps to improve on them?

6. What is stable sorting and why is it important in radix sorting? Illustrate your answer with a suitable example.

7. Describe the salient details of Figure 1 from the paper as precisely and concisely as possible. That is, convey the important points without using the figure. Repeat for Figure 2.

8. How does the paper's implementation of GPU radix sort take advantage of the GPU *shared memory*?

9. Describe *sorting by 1-bit splits* and illustrate its action on the following data:

39 10 3 89 24 26 58 74 26 48